Spin hall high density array design for next generation embedded application

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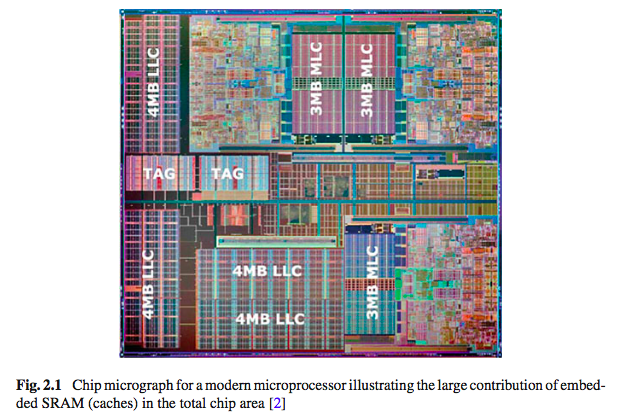
### Working time: since 8/6/2016

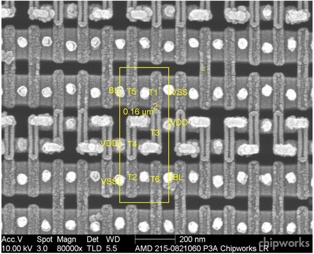
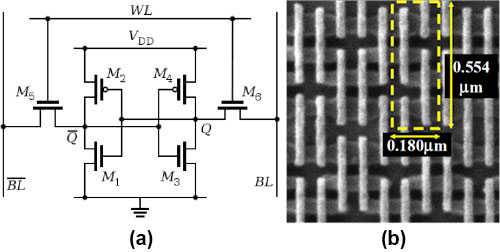
### Disclosure and conferenc paeper writing

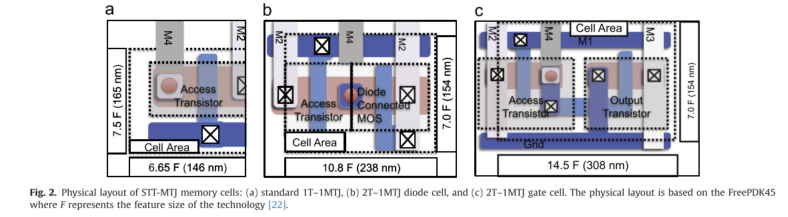
* [ ] Concept forming
* [ ] Passing through the writing block
* [ ] Finishing the drafting
* [ ] Getting feedback from the related person.
* [ ] Data and information searching

### Motivation

* Future direction of MRAM design for shrinking the Cache memory
* Non of the NVM memory could possibilily compete with MRAM structures
* MRAM show up in the embedded system in 2017, 2018 in low power high performance consumer product (Apple Watch).
* More demanding and investment for enhancing MRAM technology into maturity.
* ReRAM would struggle for getting a space for embedded technology and also losing to 3D NAND technology.
* Spin Hall material is coming to maturity.
* Using external transistor to reduce keeping the large Vsense.
* Hybrid SCM/DRAM with NAND structure will be likely to happen to lower the cost, such as NVDIMM-M
* MRAM will be embedded cache replacement, due to its high speed.
* Writing:
* **Currently, many emergening NVM system is on the track to provide faster interface with CPU. All the large semiconductor fundries will provide MRAM as standard embedded cache CPU (for example L2 chache replacement). Everspin has shipped 256Mb perpendicular magnetic tunnl junction for stand-alone memory with DDR4 interface. Now 1T1MTJ proposal has been investigated and demonstrated very mature technology for embedded technology interface with CPU. However, as the technology proceeded, it will require more demanding requirement for the next generation MRAM technology. The need for high performance speed for MRAM technology has been demonstrated.**

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(From Ref 2)

### Issues to be resolve

* Old patent didn’t address the leakage current issue.
* Read disturbance issue for crosspoint array.
* VVCMA need asymmetric correction.

### Design concept and drawing (idea disclosure)

* Using spin Hall device to reduce device layout area for embedded memory cache application.
* Due to external transistor size, additional area is needed. More embedded high density NVM memory is needed.
* Need OTS implementation for read improvement for large array.
* future neuro-network-based.
* Asymmetric line for improving size.
* Non-linear implemntatin for MRAM, such as amourphouse silicon technology. PN junction to futher improve the
* Patent reference:
* Two Cornell’s patent
* two of my spin hall papers
* Large transistor design to provide enough power for fast read.
* Asymmetric bit line design for offsetting VVCMA for the last bit.
* Vread problem for the last bit and matrix compensation.
* Double MgO free layer design with spin hall structure for sythentic free Spin Hall MRAM design
* Cross-point structure could possible introduce logic operation with magnetic logic operation and support nerophofic computation.
* **Here, we propose a novel design for MRAM to future reduce cache technology with improve read process to reduce the requirement. Here, we implement the analysis from ReRAM crosspoint and add non-linear component to expand the array for MRAM. In this analysis, we further propose the simple implementation for high density array MRAM for next generation for high speed read and write operation for MRAM.**

### Analysis details:

# 28nm node TSMC technology

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Physical Spin Hall system parameters |  |  |  |  |  |
| Array size | 1x1 |  |  |  |  |
| Line material | Pt | beta-W | Ta | CuBi,CuIr |  |
| SHE angle | 0.07 | 0.33 | 0.12 |  |  |
| Interface stack | Pt | W/Hf |  |  |  |
| Thermal stability | 60 |  |  |  |  |
| Material resistivity(uOhm-cm) |  | 260 |  |  |  |
| Jcwrite(A/cm2) | 108 |  |  |  |  |
| MTJ device | 20nm x 20nm |  |  |  |  |
| Resistance area product (RA) (ohm\*um2) | 10 |  |  |  |  |
| RHRS(kOhm) |  |  |  |  |  |
| RLRS (kOhm) | 10 |  |  |  |  |
| Line width | 28nm |  |  |  |  |
| Line thickness | 6nm |  |  |  |  |
| Line resistance |  |  |  |  |  |

# Write Operation

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Design parameters |  |  |  |  |  |
| Write operation |  |  |  |  |  |
| Vwrite (mA) | left | nicely | right |  |  |
| VVCMA |  |  |  |  |  |
| Iwrite |  |  |  |  |  |

# Read Operation

|  |  |  |  |
| --- | --- | --- | --- |
| Design parameters | 1x1 |  |  |
| Array size |  |  |  |
| Line material | Pt | W | Ta |
| SHE angle | 0.07 | 0.33 | 0.12 |
| Interface stack | Pt | W/Hf |  |

Key parameter form HGST spec for ReRAM/OTS design   
|Key parameter|

### To FIND: Information and Spec to look up on line

* [ ] Pt resistivity
* [ ] Transistor deisng power and current voltage strength
* [ ] Current exciting design
* [ ]
* [ ]

### To DO: Draw CAD draw for circuit design

* [ ] MRAM embedded ASIC performance, and peformance chart for MRA
* [ ] Magnetic-based logic operation

### To be DRAW: Illusion to be included in draft

* [X] standard L2-cache SRAM design with 6T transistor connection
* [ ] Layout design for 1T1MTJ transistor desig
* [ ] Internal illustration for MRAM design.

### Reference

* Luqiao’s crosspoint patent[1]
* Patrick crosspoint patent for structure
* Standford Philips Wang cross point estimation
* 1T1MTJ stats of art results
* Jongyeon Kim two patent disclosure
* Jongyeon Kim’s paper about spin torque logic.

[1]: Liu, L. et al. Spin-torque switching with the giant spin Hall effect of tantalum. Science 336, 555–8 (2012).

[2]: Patel, R., Ipek, E. & Friedman, E. G. 2T-1R STT-MRAM memory cells for enhanced on/off current ratio. *Microelectronics J.* **45,** 133–143 (2014).